REMARKS

Claims 1-11 and 14-20 are pending in the application.

Claims 1-3, 5-11, and 14-20 stand rejected.

Claim 4 stands objected to.

Claim 9 has been amended.

Claim Objections

Claim 4 was objected to as being dependent upon a rejected base claim but was indicated as being allowable if rewritten in independent form. Applicants thank the Examiner for the consideration of this claim. Applicants believe that claim 4 is currently allowable by virtue of depending upon an allowable base claim. Applicants will rewrite this claim in independent form at a later point in prosecution, if necessary.

Amendments to Drawings

FIGs. 1 and 2 have been amended to delete reference numerals 12 and 13 respectively. Additionally, FIG. 1 has been amended to replace reference numeral 17, used to describe the TX flow control signal, with reference numeral 60. The detailed description has been amended to reflect the use of reference numeral 60.

Rejection of Claims under 35 U.S.C. §112

Claim 9 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claim 9 for clarification purposes only. Applicant notes that this amendment does not narrow the scope of claim 9.

Rejection of Claims under 35 U.S.C. §102

Claims 1, 3, 6, 7, and 9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ishikawa, U.S. Patent No. 5,748,018 (Ishikawa). Applicants respectfully traverse this rejection.

A similar rejection was maintained in the earlier Office Action, mailed September 30, 2002. In that Office Action, the Examiner contended that Ishikawa teaches "a register having a first input for receiving a data signal, a second input for receiving a clock signal, and an output; and a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register", as recited in claim 1. In particular, the Examiner stated that D-FF (D-Flip Flop) 101 and buffer 103 of Ishikawa respectively teach the register and buffer recited in claim 1. Office Action, September 30, 2003, pp. 2-3.

As noted by Applicants in their previous response (mailed February 20, 2004), at col. 4, lines 14-33, Ishikawa recites:

> Referring to FIG. 2B, there is shown a timing chart illustrating an operation of the data output circuit shown in FIG. 2A. In addition, "assuming that an internal delay time of the D-FF 101 as compared with the external clock signal CLK is t_q, and a delay time of the output buffer 102 as compared with the output of the D-FF 101 is t_b, a delay time t_d in the data transfer as compared with the external clock CLK is expressed as $t_q + t_b$. On the other hand, assuming that a difference in time between the external clock signal CLK and the delayed clock signal CLKD is t_b, a delay time t_D in the data transfer as compared with the delayed clock CLKD is expressed as follows:
>
> $t_D = t_q + t_b - t_b = t_q$
>
> Accordingly, the delay time t_D in the data transfer becomes equal to t_q, and therefore, this becomes substantially equivalent to the fact that the internal clock signal is advanced as compared with the external clock by the time t_b by using the PLL circuit.

Ishikawa also teaches that the data transfer can be executed within Tcycle "if the delay time t_{B103} of the output buffer 103 is set to a value not smaller than $\{t_s + t_q + t_b -$ Tcycle$\}$". Ishikawa, col. 5, lines 14-28. Accordingly, Ishikawa neither teaches nor suggests making the delay of buffer 103 (which the Examiner relies on to teach the "buffer" of claim 1) substantially equivalent to the delay of D-FF 101 (which the Examiner relies on to teach the "register" of claim 1).

The Examiner also relies upon FIG. 2B. As also noted in Applicants' previous response, FIG. 2B does not teach a buffer with a delay equal to the delay of a register. In FIG. 2B, the quantity tq+tb appears to be more than twice the length of t_b, suggesting that t_b and t_q are not equal. Additionally, the timing diagram of FIG. 2B is not drawn to any particular scale, and thus one of ordinary skill in the art could easily interpret any apparent correlation between t_q and t_b as a coincidence, especially given that none of the cited portions of the reference suggest such a relationship between these two quantities. This is especially true in light of the fact that t_b and t_{b103} are not drawn the same size in FIG. 2B, despite the fact that the claims of Ishikawa recite that these quantities are equal.

In the current Office Action (mailed May 24, 2004), the Examiner also relies upon the timing diagram shown in FIG. 3B of Ishikawa to show that "the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D". As with FIG. 2B, FIG. 3B is not drawn to any particular scale, and thus Applicants assert that any apparent similarities would not have suggested anything to one of ordinary skill in the art, especially given that no other portion of the reference teaches or suggests such similarities. Furthermore, even assuming that FIG. 3B is drawn to scale, the quantity labeled t_{B103} is perceptively smaller (1.25 cm in Applicants' copy of the reference) than the quantity labeled T_D (1.5 cm in Applicants' copy of the reference). Given that the scale of the drawing is not labeled, the drawing does not show the quantities as being the same size, and no other teaching or suggestion that these quantities are "substantially equal" has been provided, Applicants assert that the reference simply does not teach or suggest this feature of claim 1.

In the Response to Arguments section of the current Office Action (mailed May 24, 2004), the Examiner states that, "in col. 11, lines 35-38, Ishikawa further discloses the buffer 103 generating a delay clocked signal by a delay amount equal to the delay amount of register 101." This portion of Ishikawa refers to a portion of claim 1 of Ishikawa, which recites: "said data output circuit comprising a data outputting means... and a clock delay means... for outputting a delayed clock signal which is delayed from said external clock signal by a delay amount equal to a data delay amount of said data outputting means." Applicants note that "data outputting means", as referred to in claim 1 of Ishikawa, does not teach or suggest a register. This conclusion is made more clear when claim 3 of Ishikawa is considered. Claim 3, which depends from claim 1, recites that

"the data output circuit further includes a D-type flipflop... and said data outputting means is constituted of a first output buffer having an input connected to a data output of said D-type flipflop." Clearly, Ishikawa teaches that the data outputting means can be a buffer, that a flip flop can be coupled to that buffer, and that the delay of the buffer, which constitutes the "data outputting means", equals the delay of the "clock delay means". Just as clearly, however, Ishikawa does not teach or suggest a "a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register" as recited in claim 1 of the present invention. For this reason, the cited art fails to anticipate, teach, or suggest claim 1.

Further with respect to claim 1, Applicant notes that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). As noted in the previous response, the cited art fails to teach or suggest "a source clock domain in a first network protocol layer" and "a destination clock domain in a second network protocol layer", as recited in claim 1. The Examiner cites the data output circuit 100 of FIG. 3A of Ishikawa as being "a first layer" and the data input circuit 200 in the same figure as being "a second layer." However, these circuits are clearly not implementing network protocol layers (in fact, none of the terms "network", "layer", or "protocol" are used in Ishikawa). Since these features of claim 1 are neither taught nor suggested in the cited art, Applicant requests the withdrawal of this rejection.

In the Response to Arguments section of the current Office Action, the Examiner states that, "Though Ishikawa does not disclose for the terms 'network', 'layer', or 'protocol', the circuits 100 and 200 still read on them for the following reasons. These terms in the claim context has no structure or function that would enable them to distinguish from circuits 100 and 200. Thus, the broadest interpretation is given to the claims." Office Action, p. 8.

In response to these statements, Applicants first note that "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re*

Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (C.C.P.A. 1970). Thus, if the Examiner's "broadest interpretation" fails to take the terms "network", "layer", and "protocol" into consideration, the alleged broadest interpretation is an invalid interpretation. Additionally, the Examiner's assertion that the terms "first network protocol layer" and "second network protocol layer" have "no structure or function" is simply untrue. As one of ordinary skill in the art would recognize, network protocol layers are used to provide specific functionality. This functionality is neither taught nor suggested by the cited art, as would be expected, given that the cited reference does not address networking. Accordingly, Applicants respectfully respect withdrawal of this rejection.

Additionally, it is unclear what is meant by the Examiner's statement that the prior art "read[s] on" Applicant's claim. Applicants note that the proper concern is whether Applicants' claim reads on the prior art, not vice versa. For example, the fact that prior art claims may be broad enough the read on the claimed invention does not support a conclusion of obviousness. *See In re Benno*, 768 F.2d 1340, 1345-46, 226 USPQ 683, 686 (Fed. Cir. 1985) and *In re Vamco Mach. & Tool, Inc.*, 752 F.2d 1564, 1577, n.5, 224 USPQ2d 617, 625, n.5 (Fed. Cir. 1985)).

Applicant requests the withdrawal of the rejection of claims 3, 6, 7, and 9 for reasons similar to those provided above with respect to claim 1.

Additionally with respect to claim 9, as noted in Applicants' previous response (mailed February 20, 2004), the cited art fails to teach or suggest "receiving an input clock signal in a first clock domain in a first layer; receiving an input data signal in the first clock domain in the first layer; latching the input data signal by triggering the input data signal by the input clock signal; [and] delaying the input clock signal by an amount that is equal to the delay in the latching", as recited in claim 9 (emphasis added). Applicant notes that this claim recites that the input clock signal is delayed by an amount that is equal to the delay in the latching. Given the above reasons why the cited art fails to teach a buffer generating a delay that is substantially equivalent to a delay through a register, the cited art clearly fails to teach or suggest delaying the input clock signal by an amount that is equal to the delay in the latching. Claim 14 is patentable over the cited art for similar reasons.

Rejection of Claims under 35 U.S.C. §103

Claims 2, 10, 11, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ishikawa, U.S. Patent No. 5,748,018 (Ishikawa). Applicants respectfully traverse this rejection, for at least the foregoing reasons provided with respect to claim 1.

In the current Office Action, the Examiner states that, despite the fact that "Ishikawa fails to teach said first layer comprising a link layer and said second layer comprising a PHY layer" (Office Action, p. 5), "it would have been obvious to a person of ordinary skill in the art to arrange the source synchronous clocking system between the link layer and the physical layer instead in an IC circuit, since such arrangement is a matter of choice serving the same purpose."

Applicants note that, in order to support a §103 rejection, the Examiner must provide a factual basis. *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 177-78 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). Accordingly, the Examiner's opinion that a limitation is a "matter of choice" is not a proper basis of rejection, since this statement clearly does not provide a factual basis for the rejection. Furthermore, the Board has held that examiners have misstated the law by "equating that which is within the capabilities of the skilled designer with obviousness." *In re Sung Nam Cho*, 813 F.2d 378. Therefore, the rejection of claim 2 is improper.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on **June 30, 2004**.

Brenna A Brock 6-30-2004
Attorney for Applicant Date of Signature

Respectfully submitted,

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ANNOTATED SHEET SHOWING CHANGES

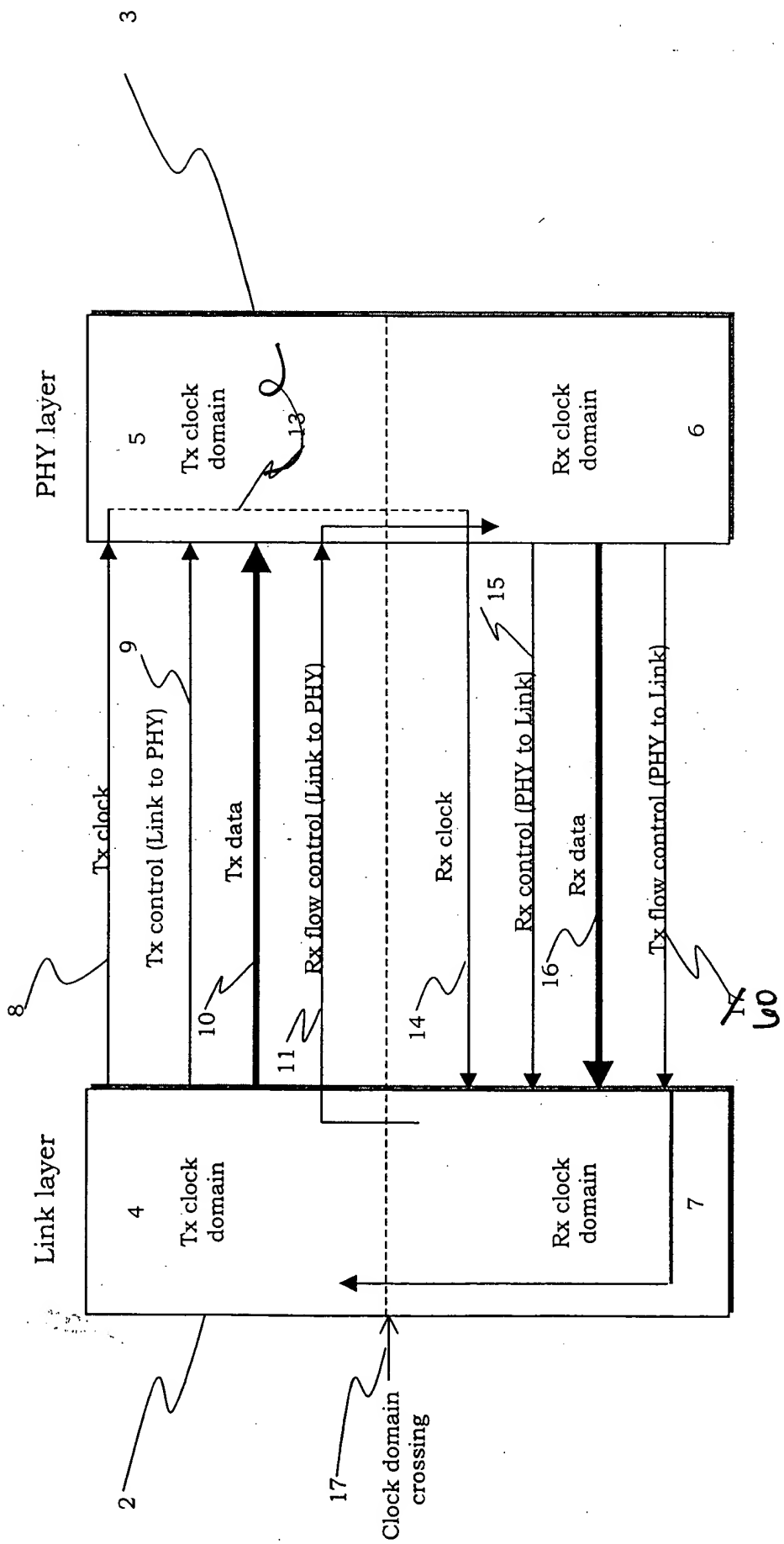

FIGURE 1

ANNOTATED SHEET SHOWING CHANGES

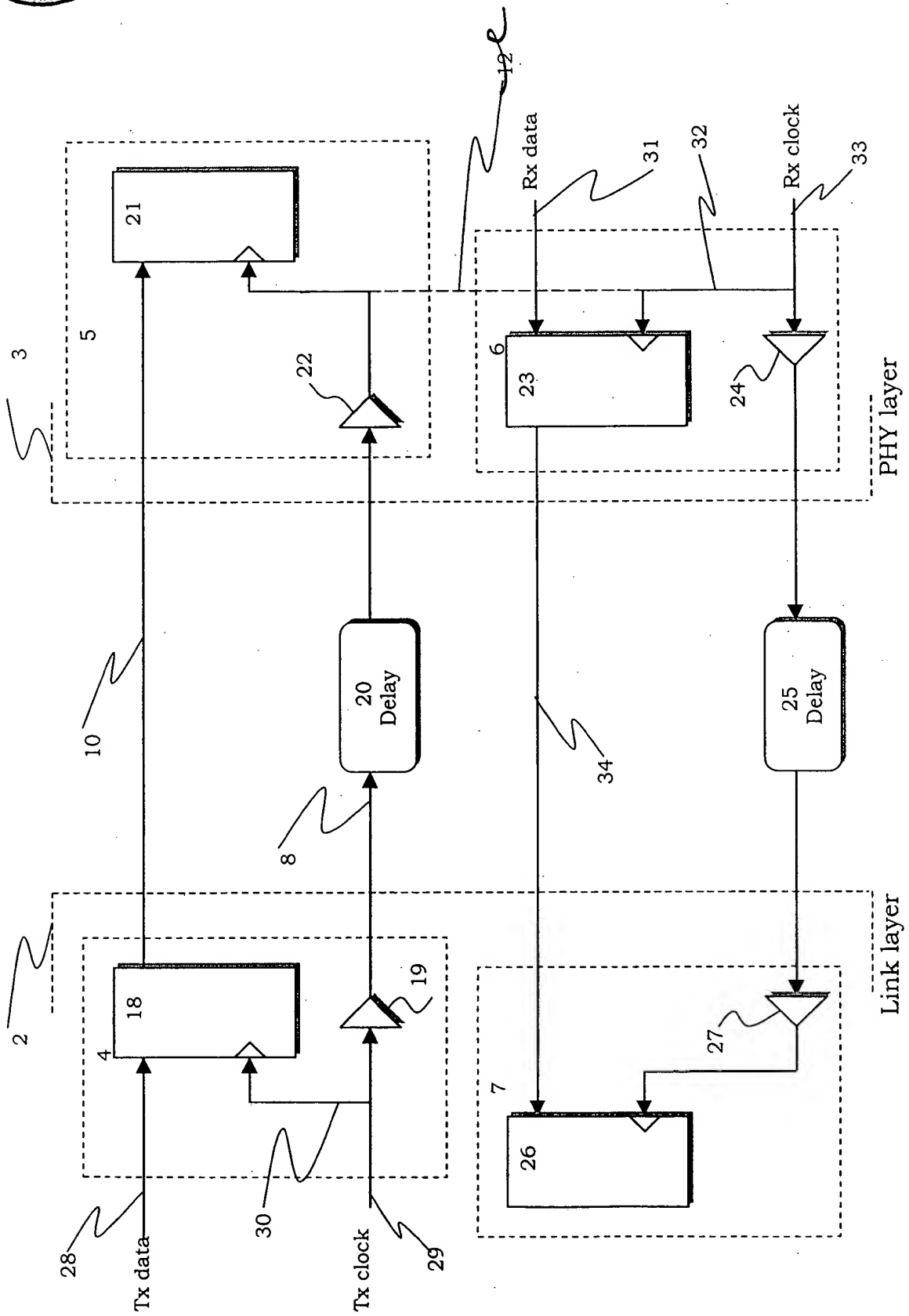

FIGURE 2